

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	3131051	memory or storage	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/06/08 15:49
L2	31013	1 and (bit or bitline) near3 (switch\$5 or transistor)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/06/08 15:52
L3	2335	2 and (detect\$5 or monitor\$5 or compar\$5) with current with (bit or bitline)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/06/08 16:04
L4	18	3 and (compensat\$5 or maintain\$5) with (voltage or potential or level) near2 drop with (switch\$5 or transistor)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/06/08 15:57
L5	411	3 and (regulat\$5 or maintain\$5) with (voltage or potential or level) with (bit or bitline)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/06/08 16:09
L6	404	5 and (voltage or potential or level) with (switch\$5 or transistor)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/06/08 16:10
L7	280	5 and (voltage or potential or level) with (switch\$5 or transistor) with (power or supply or (voltage or potential) adj2 generat\$5)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/06/08 16:12
L8	156	7 and (compensat\$5 or adjust\$5)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/06/08 16:36
L9	45	8 and mirror\$5 and ratio with current	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/06/08 16:38
L11	22	9 and chang\$5 with resistance	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/06/08 16:39

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L1	3131051	memory or storage	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/06/08 09:33
L2	5094	1 and voltage adj2 drop with switch\$5	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/06/08 09:25
L3	160	1 and voltage adj2 drop with switch\$5 with regulator	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/06/08 09:29
L4	8	3 and current with (bit or bitline)	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/06/08 09:22
L5	160	1 and voltage adj2 drop with switch\$5 with regulator	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/06/08 09:26
L6	7	5 and (bit or bitline) near3 current	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/06/08 09:30
L7	171	1 and voltage adj2 drop with transistor with regulator	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/06/08 09:29
L8	7	7 and (bit or bitline) near3 current	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/06/08 09:30
L9	23	1 and compensat\$5 with (voltage or potential or level) near3 drop with (switch\$5 or transistor) with regulat\$5	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	ON	2005/06/08 09:35